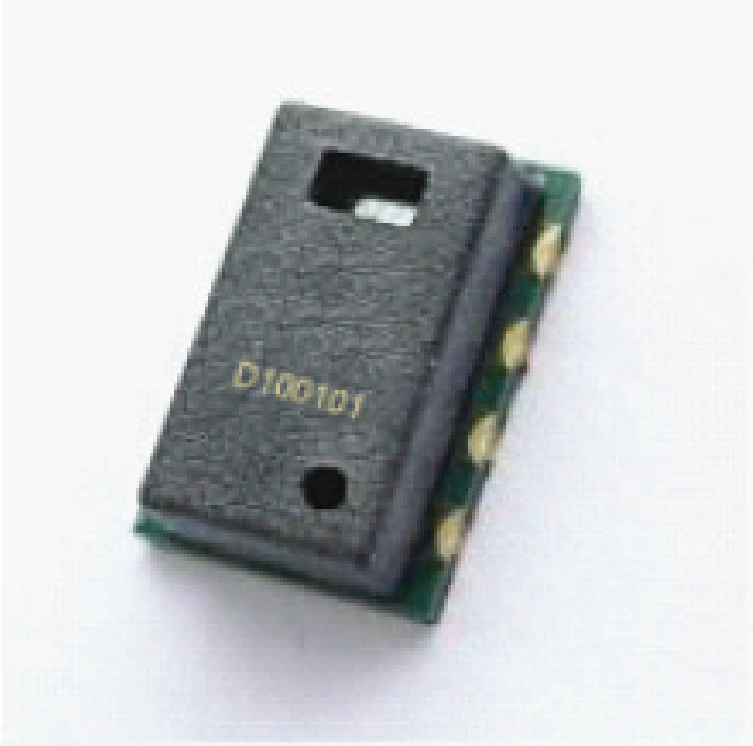
GE
Measurement & Control

Advanced Sensors

ChipCap 2®

Application Guide



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916-127 Rev. A
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1. General Information

1.1 Preliminary Consideration

To maximize the performance of ChipCap 2, it is important to plan an appropriate location of the sensor at the design stage. Airflow and proper exposure to ambient air must be secured for ChipCap 2 to ensure expected performance. Airflow holes must NOT be blocked. Any heat generating parts near ChipCap 2 will distort the proper measurement of relative humidity and temperature reading, and heat generating parts should be avoided or measures should be taken to prevent heat transfer.

1.2 Operating Conditions

Figure 1 below shows ChipCap 2‘s maximum and recommended normal operating condition. Within the normal range, ChipCap 2 performs in a stable manner. Prolonged exposures to conditions outside normal range, especially at humidity over 90%RH, may temporarily offset the RH signal up to ±3%RH. When it returns to the normal range, it will gradually recover back to the calibration state.

The re-conditioning procedure in section 1.6 on page 3 will help reduce this recovery time. Long term exposure to extreme conditions may also accelerate aging of the sensor.

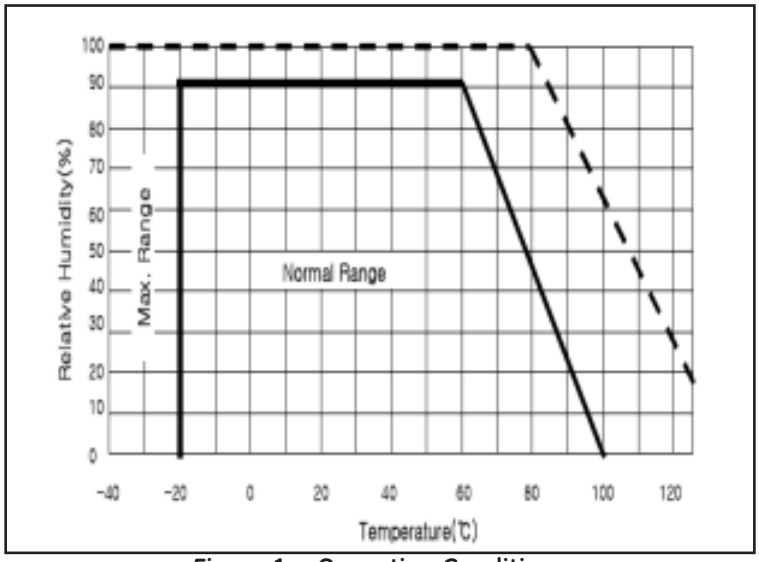


Figure 1: Operating Conditions

1.3 Heating

Though within the accuracy tolerance, self-heating in the sensor IC may affect accurate measurement of temperature and RH%. The measurement error from self heating can be reduced by keeping “Active State” to the minimum, and by regulating the operating voltage within 3.3 ±0.5V, 5.0 ±0.5V. A sampling time of more than 200ms is recommended for measurement.

Other heat sources such as power electronics, microcontrollers, and display near the sensor may affect the accurate measurement. Sensor location near such heat sources should be avoided by maintaining distance or a thermal buffer. A thin metal pattern, or even better, “milling slits” around the sensor also may help reduce the error.

1.4 Soldering Instruction

ChipCap 2 is designed for a mass production reflow soldering process. It is qualified for soldering profile according to IPC/JEDEC J-STD-020D (see Figure 2 below) for Pb-free assembly in standard reflow soldering ovens or IR/Convection reflow ovens to withstand peak temperature at 260°C and peak time up to 40 sec. For soldering in Vapor Phase Reflow (VPR) ovens, the peak conditions are limited to T_P < 240°C with t_P <40sec and ramp-up/down speeds shall be limited to 10°C/sec. For manual soldering, contact time should be limited to 5 seconds at up to 350°C. No-Clean solder flux should be used.

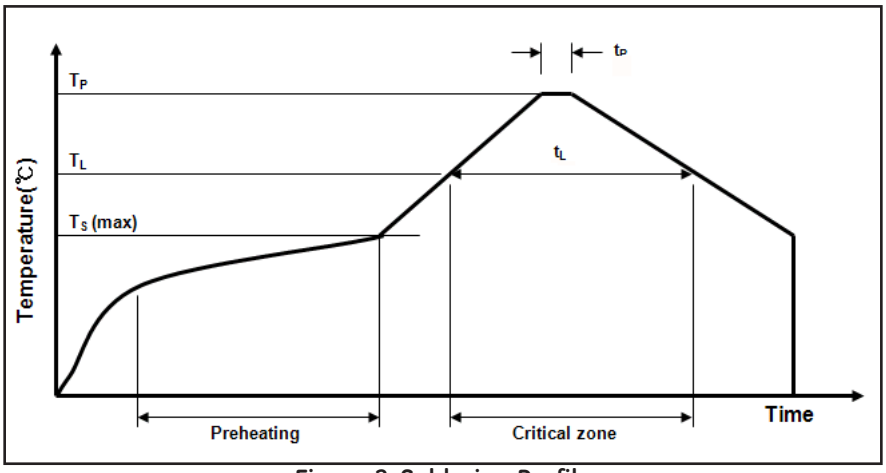


Figure 2: Soldering Profile

JEDEC standard
$T_P \leq 260°C$, $t_P < 40sec$, $T_L < 220°C$, $t_L < 150sec$.
Ramp-up/down speed < 5°C/sec.

IMPORTANT: *Test or measurement right after reflow soldering may read an offset as the sensor needs time for re-hydration. The recovery time may vary depending on reflow soldering profile and ambient storage condition.*

For most of the standard reflow soldering, the following rehydration process will bring the sensor back to less than ±1%RH of the original calibration state.

Re-hydration: 30 ±5°C, 80 ±5%RH, Duration: 60 hrs

Contact GE customer support for customized recovery measures specific to your reflow soldering process.

For Land Pattern drawing and dimensions, see Figure 4 on page 4.

1.5 Storage and Handling Information

ChipCap 2 contains a polymer based capacitive humidity sensor sensitive to environment, and should NOT be handled as an ordinary electronic component.

Chemical vapors at high concentration may interface with the polymer layers, and, coupled, with long exposure time, may cause a shift in both offset and sensitivity of the sensor.

Although the sensor endures the extreme conditions of -50°C~150°C, 0%~100%RH (non condensing), long term exposure in such an environment may also offset the sensor reading. Hence, once the package is opened, it is recommended to store it in a clean environment with temperature at 5°C~55°C and humidity at 10%~70%RH.

ChipCap 2 is ESD protected up to 4000V and has Latchup of ±100°C or (up to +8V / down to -4V) relative to VSS/VSSA, and is also packed in ESD protected shipping material. Normal ESD precautions are required when handling in the assembly process.

1.6 Reconditioning Procedure

If ChipCap 2 is exposed to extreme conditions or contaminated with chemical vapors, the following reconditioning procedure will recover the sensor back to calibration state.

Baking: 120°C for 3 hrs and

Re-Hydration: 30±5°C at 80 ±5%RH for 60 hrs

1.7 Material Contents

ChipCap 2 consists of a sensor cell and IC (polymer /glass and silicon substrate) packaged in a surface mountable LCC (Leadless Chip Carrier) type package. The sensor housing consists of a PPS (Poly Phenylene Sulfide) cap with epoxy glob top on a standard FR4 substrate. Pads are made of Au plated Cu. The device is free of Pb, Cd and Hg.

A RoHS compliant / REACH report is available.

1.8 Traceability Information

ChipCap 2 is laser marked with product type and lot identification. Further information about an individual sensor is electronically stored on the chip.

The first line denotes the sensor type: CC2-A for PDM output, CC2-D for I²C output.

Lot identification is printed on the second line with a 5 digit alphanumeric code.

An electronic identification code stored on the chip can be decoded and allows for tracking on a batch level through production, calibration and testing.

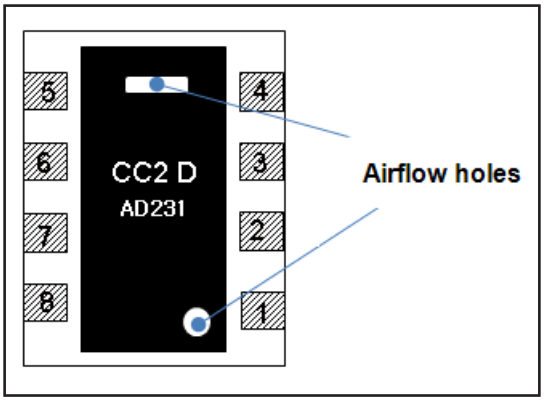


Figure 3: Laser Marking

1.9 Shipping Package

ChipCap 2 is provided in tape and reel shipment packaging, sealed into antistatic ESD trays. Standard packaging sizes are 2,500 or 500 units per reel. The drawing of the packaging tapes with sensor orientation and packing box dimensions are shown in Figure 4 below and Figure 5 on the next page.

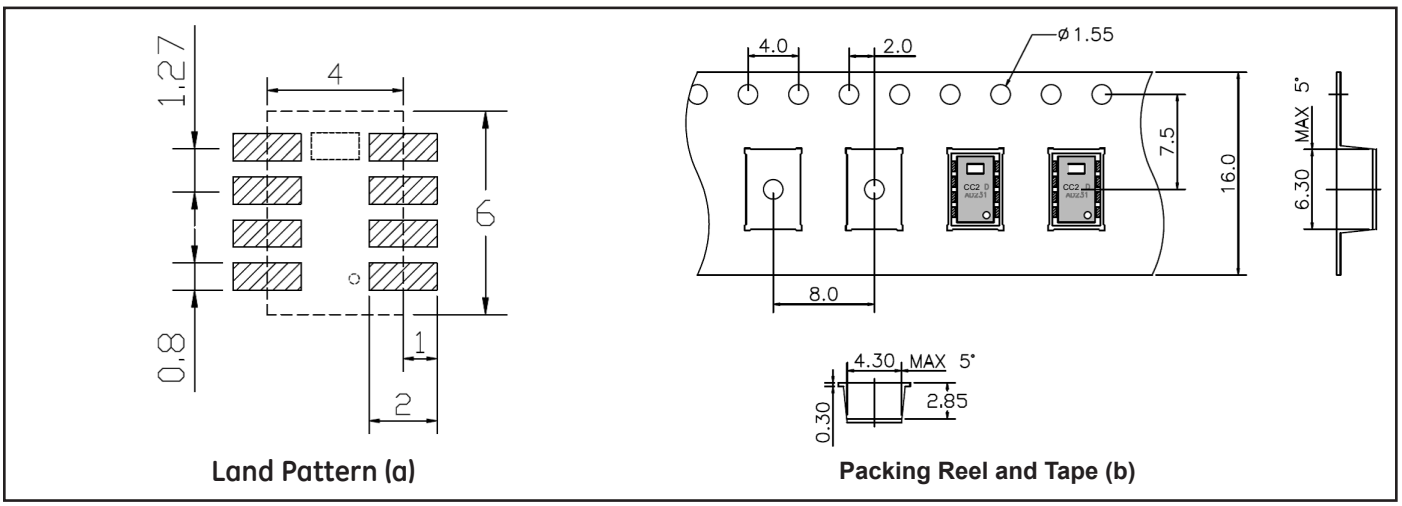
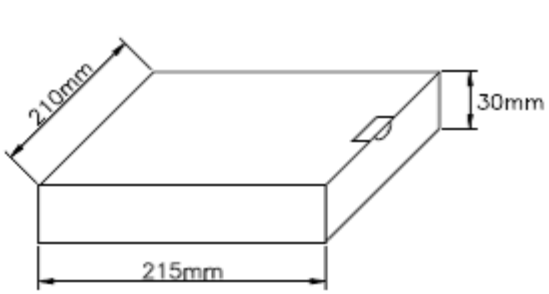
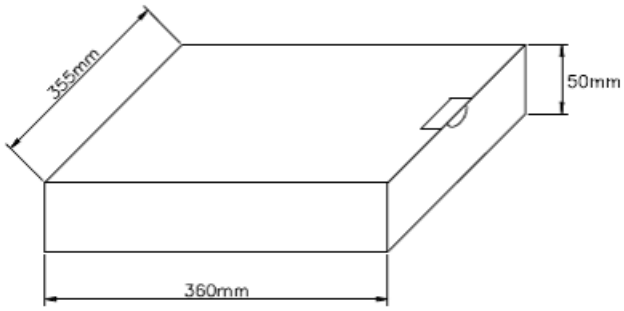


Figure 4: Packaging Tapes

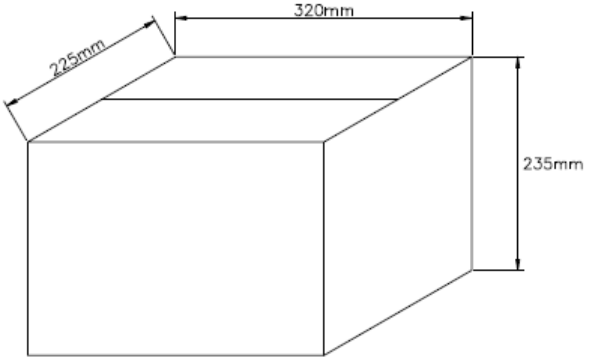
1.9 Shipping Package (cont.)



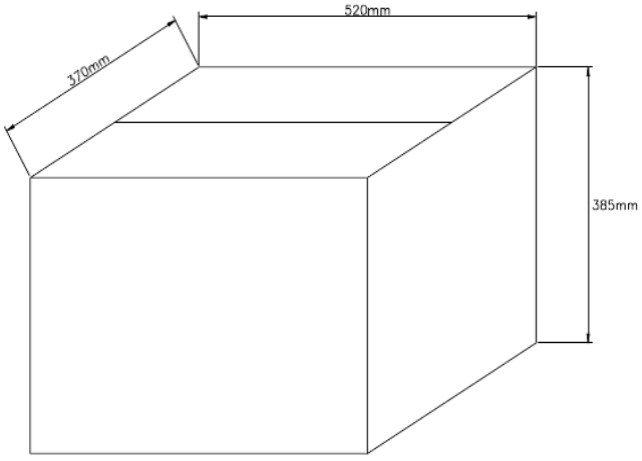
Inbox: 500 ea
Dimension: 215 x 210 x 30 mm



Inbox: 2,500 each
Dimension: 360 x 355 x 50 mm



Outbox: 5,000 each (5 x Inbox 500)
Dimension: 320 x 225 x 235 mm



Outbox: 25,000 each (10 x Inbox 2500)
Dimensions: 520 x 370 x 385 mm

Figure 5: Packing (Box)

2. Interface Specification

2.1 Digital Output (I²C Interface)

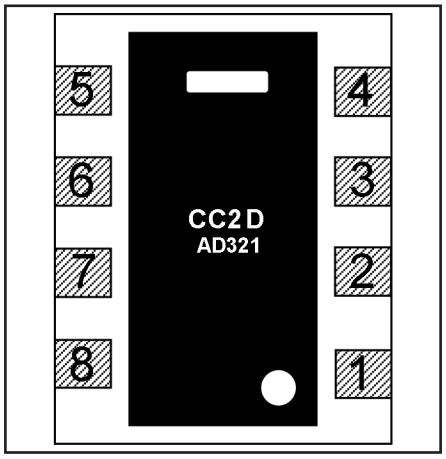


Figure 6: Pin Assignments

Table 1: Pin Assignments

Pin-No	Name	Description
1	Alarm_Low	Low alarm output
2	Ready	Ready signal (conversion complete output)
3	SDA	I^2C data
4	SCL	I^2C clock
5	V_{CORE}	Core voltage
6	VSS	Ground supply
7	VDD	Supply voltage (2.7-5.5V)
8	Alarm_High	High alarm output

2.1.1 Power Pads (5.V_{CORE}, 6.VSS, 7.VDD)

ChipCap 2 is capable of operating on a wide range of power supply voltages from 2.7V to 5.5V.

The recommended supply voltage is either 3.3 ±0.5V or 5.0 ±0.5V. The power supply should be connected to VDD (power supply pad 7). VDD and VSS (Ground pad 6) should be decoupled with a 220nF capacitor.

IMPORTANT: *V_{core} must not be connected to VDD, and it must always be connected to an external 100nF capacitor to ground. (see Figure 7, "Typical Application Circuit (I2C)," on page 7).*

2.1.2 Serial Clock & Data Pads (3. SDA, 4. SCL)

The sensor's data is transferred in and out through the SDA pad, while the communication between ChipCap 2 and the microcontroller (MCU) is synchronized through the SCL pad.

ChipCap 2 has an internal temperature compensated oscillator that provides time base for all operation, and uses an I²C-compatible communication protocol with support for 100 KHz to 400 KHz bit rates.

External pull-up resistors are required to pull the drive signal high; they can be included in the I/O circuits of microcontroller.

Further information about timing and communication between the sensor and microcontroller is explained in Section 4, "Communicating with ChipCap 2" on page 13.

2.1.3 Alarm Pads (1. Alarm Low, 8. Alarm High)

The alarm output can be used to monitor whether the sensor reading has exceeded or fallen below pre-programmed values. The alarm can be used to drive an open-drain load connected to VDD, or it can function as a full push-pull driver. If a high voltage application is required, external devices can be controlled with the Alarm pins, as demonstrated in Figure 21 on page 30

The two alarm outputs can be used simultaneously, and these alarms can be used in combination with the I²C. Further information about alarm control is explained in Section 6.

- VDD and Ground is decoupled by a 220nF capacitor.
- Vcore (Not Used) and Ground is decoupled by 100nF capacitor.
- Pull-up resistors should be included between ChipCap 2 and MCU.

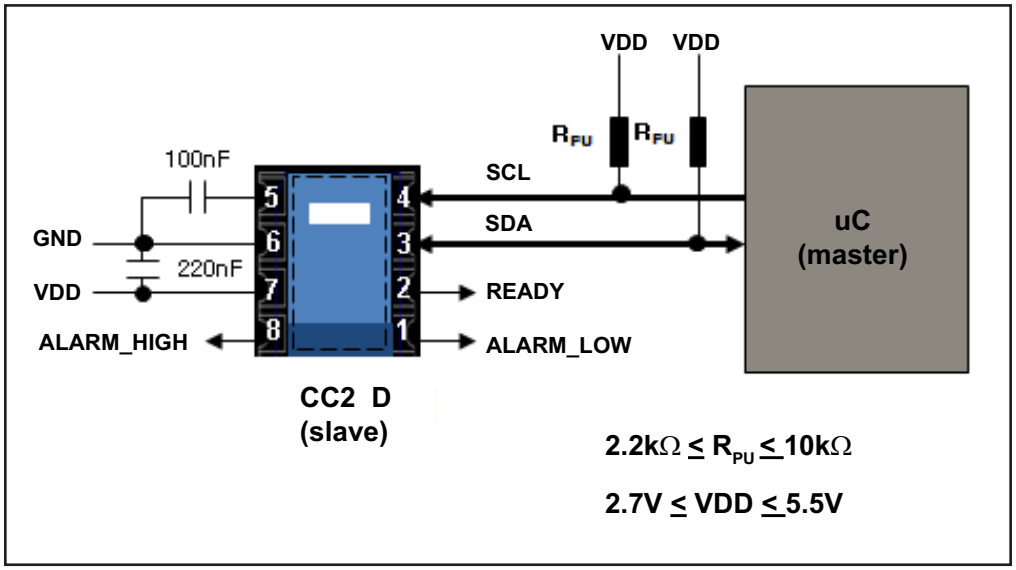


Figure 7: Typical Application Circuit (I²C)

2.2 Analog Output (PDM)

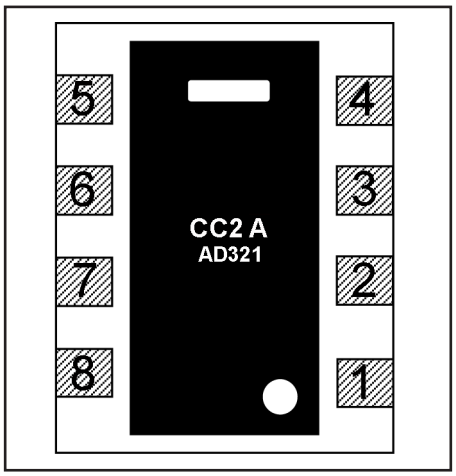


Figure 8: Pin Assignments

Table 2: Pin Assignments for Analog Output

Pin-No	Name	Description
1	PDM_T	Temperature PDM
2	PDM_H	Humidity PDM
3	SDA	I^2C data (Not Used)
4	SCL	I^2C clock (Not Used)
5	V_{CORE}	Core voltage
6	VSS	Ground supply
7	VDD	Supply voltage (2.7-5.5V)
8	Alarm_High	High Alarm output

2.2.1 Power Pads (5.VCORE, 6.VSS, 7.VDD)

ChipCap 2 is capable of operating on a wide range of power supply voltages from 2.7V to 5.5V. The recommended supply voltage is either 3.3 ±0.5V or 5.0 ±0.5V.

The power supply should be connected to VDD (power supply pad 7). VDD and VSS (Ground pad 6) should be decoupled with a 220 nF capacitor.

IMPORTANT: *V_{core} must not be connected to VDD, and it must always be connected to an external 100 nF capacitor to ground (see Figure 9 on page 9).*

2.2.2 PDM Output Pads (1.PDM_T, 2.PDM_H)

Temperature PDM (Pulse Density Modulation) appears on the PDM_T/Alarm_Low pad (1) and corrected Humidity PDM appears on the PDM_H pad (2).

When pad (1) is selected for Temperature PDM, the Alarm_Low function is disabled and only one Alarm function (Alarm_High: pad 8) is usable.

Note: *The ChipCap 2 PDM output is pre-programmed in the factory for Humidity and Temperature output mode.*

2.2.3 Alarm Pads (8.Alarm_High, 1.Alarm_Low [optional])

As ChipCap 2 PDM is factory set for Humidity and Temperature output mode, only the High Alarm output can be used in combination with ChipCap 2 PDM.

If both high and low alarm functions are required, pads 1 and 8 will be programmed at factory to use as Alarm_Low and Alarm_High respectively with required high and low humidity values. In such a case, ChipCap 2 will output the corrected humidity PDM only, See Section 6 for the alarm function.

2.2.4 Serial Clock & Data Pads (3.SDA, 4.SCL)

For ChipCap 2 PDM output, both SDA and SCL pads are not used and must be connected to VDD.

2.2.5 Typical Circuit Connection

VDD and Ground are decoupled by a 220nF capacitor. V_{core} (Not Used) and Ground are also decoupled by a 100nF capacitor. SCL and SDL (not used) are connected to VDD.

Between ChipCap 2 and MCU (µC), Low Pass Filtering (see Section 5.2 on page 26 for more information) with 10 kΩ resistors and 6,400 nF capacitors is added to create an analog signal.

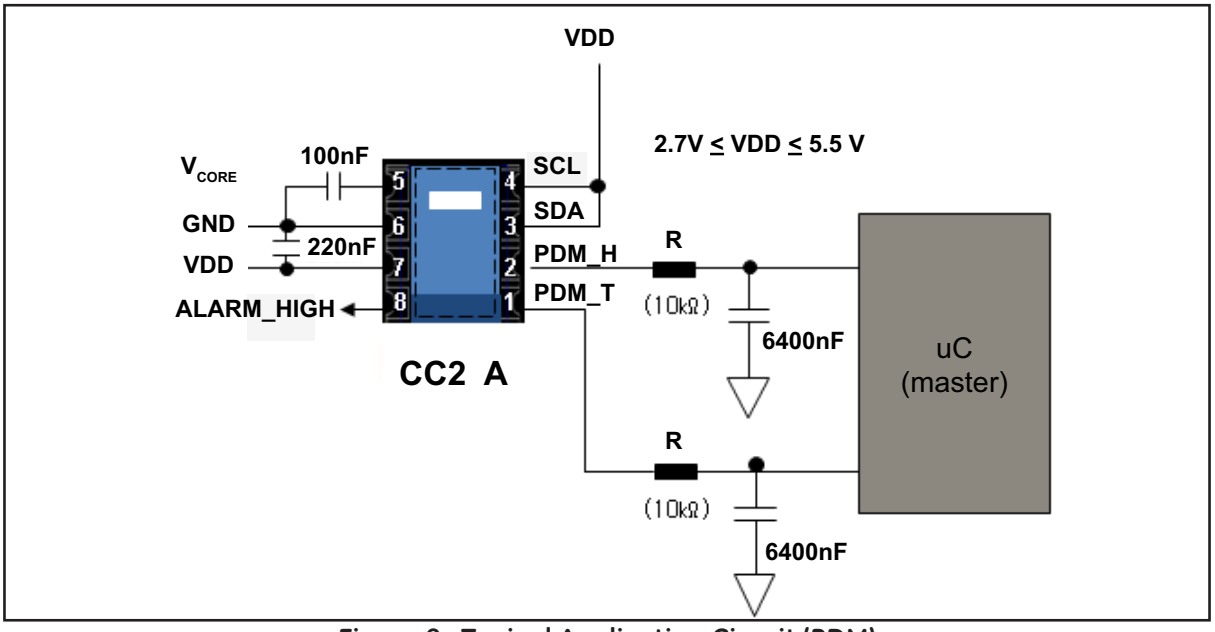


Figure 9: Typical Application Circuit (PDM)

3. Electrical Specification

3.1 Absolute Maximum Rating

Table 3 below shows the Absolute Maximum Ratings for ChipCap 2. Exposure to these extreme condition for extended period may deteriorate the sensor performance and accelerate aging. Functional operation is not implied at these conditions.

Table 3: Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Supply Voltage (V_{DD})	V_{DD}	-0.3	6.0	V
Supply Voltage at I/O pads	V_{IO}	-0.3	V_{DD}+0.3	V
Storage Temperature Range	T_{STOR}	-55	150	°C
Junction Temperature	T_j	-55	150	°C

3.2 Electrical Specification and Recommended Operating Conditions

The operating conditions recommended for ChipCap 2 are given in Table 4 and the electrical specification is shown in Table 5 on the next page.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage to Gnd	V_{SUPPLY}	2.7		5.5	V
Ambient Temperature Range	T_{AMB}	-40		125	°C
External Capacitance between V_{DD} pin and Gnd	$C_{VSUPPLY}$	100	220	470	nF
External Capacitance between Vcore and Gnd	C_{VCORE}		100		nF
Pull-up on SDA and SCL	R_{PU}	1	2.2	10	kΩ

Table 5: Electrical Characteristics Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply						
Supply Current (varies with update rate and output mode)	I_{DD}	At maximum update rate		750	1100	µA
Extra Current with PDM enabled	I_{PDM}	At maximum update rate		150		µA
Sleep Mode Current	I_{sleep}	-40 to 85°C		0.6	1	µA
		-40 to 125°C		1	3	µA
PDM Output						
Voltage Range	V_{PDM_Range}	3V±10%, 3.3V±10%, 5V±10%	10		90	$\%V_{SUPPLY}$
PDM Frequency	f_{PDM}			$f_{SYS}/8$		KHz
Filter Settling Time[1]	t_{SETT}	0% to 90% LPFilter 10kW/400nF			9.2	ms
Ripple[1]	V_{RIPP}	0% to 90% LPFilter 10kW/400nF			1.0	mV/V
PDM Additional Error (Including Ratiometricity Error)	E_{PDM}	-40 to 125°C		0.1	0.5	%
Digital I/O						
Voltage Output Level Low	V_{OL}			0	0.2	V_{SUPPLY}
Voltage Output Level High	V_{OH}		0.8	1		V_{SUPPLY}
Voltage Input Level Low	V_{IL}			0	0.2	V_{SUPPLY}
Voltage Input Level High	V_{IH}		0.8	1		V_{SUPPLY}
Total System						
Start-Up-Time , Power-on (POR) to data ready	t_{STA}	At nominal frequency; fastest and slowest settings	4.25		55	ms
Update Rate (Update Mode)	t_{RESP_UP}	Fastest and slowest settings	0.70		165	ms
Response Time (Sleep Mode)	t_{RESP_SL}	Fastest and slowest settings	1.25		45	ms

1. Please refer to section 5.2 on page 26.

3.3 Output Pad Drive Strength

The output pad drive strength at different supply voltages and operating temperatures is shown in Table 6 and Table 7 below.

Table 6: Output High Drive Strength

Output High Drive Strength (mA)						
V_{SUPPLY} (V)	-40°C		25°C		125°C	
	Min	Typ	Min	Typ	Min	Typ
2.7	7.2	10.5	5.9	8.4	4.7	6.6
3.3	12.1	16.6	9.6	12.9	7.4	10.0
5.5	20.0	20.0	20.0	20.0	20.0	20.0

Table 7: Output Low Drive Strength

Output Low Drive Strength (mA)						
V_{SUPPLY} (V)	-40°C		25°C		125°C	
	Min	Typ	Min	Typ	Min	Typ
2.7	20.0	20.0	16.0	20.0	11.7	14.9
3.3	20.0	20.0	20.0	20.0	18.2	20.0
5.5	20.0	20.0	20.0	20.0	20.0	20.0

3.4 ESD/Latch-Up-Protection

All external module pins have ESD protection of up to 4000V and latch-up protection of ±100 mA or (up to +8V/down to -4V) relative to VSS/VSSA. The internal module pin VCORE has ESD protection of up to 2000V. The ESD test follows the Human Body Model with 1.5kOhm/100 pF based on MIL 883, Method 3015.7.

4. Communicating with ChipCap 2

4.1 Power–On Sequence

On system power-on reset (POR), the ChipCap 2 wakes as an I²C device regardless of the output protocol programmed in EEPROM. After power-on reset, it enters the command window. It then waits for a Start_CM command for 10 ms if Fast Startup bit is not set in EEPROM (Factory Setting) or for 3 ms if fast startup bit is set in EEPROM (see Figure 10). If the ChipCap 2 receives the Start_CM command during the command window, it enters and remains in Command Mode.

The Command Mode is primarily used for initializing ChipCap 2.

If during the power-on sequence, the command window expires without receiving a Start_CM or if the part receives a Start_NOM command in Command Mode, the device will immediately assume its programmed output mode and will perform one complete measurement cycle.

4.2 I²C Features and Timing

The ChipCap 2 uses I²C-compatible communication protocol with support for 100kHz and 400kHz bit rates. The I²C slave address (0x00 to 0x7F) is selected by the Device_ID bits in the Cust_Config EEPROM word (see Table 16 on page 32 for bit assignments).

See Figure 11 for I²C Timing Diagram and Table 8 on page 14 for definitions of the parameters shown in the diagram.

Note: *A Detailed Timing Chart and Reference Programming Code are available upon request.*

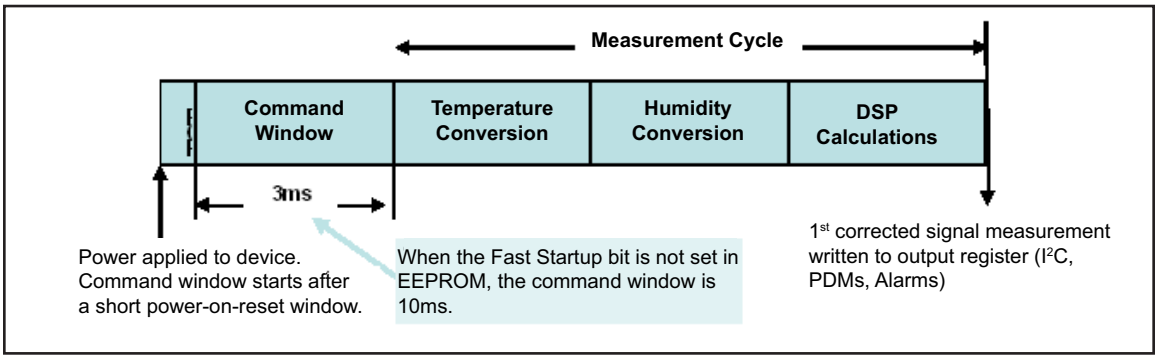


Figure 10: Power On Sequence with Fast Start-up Bit Set in EERPROM

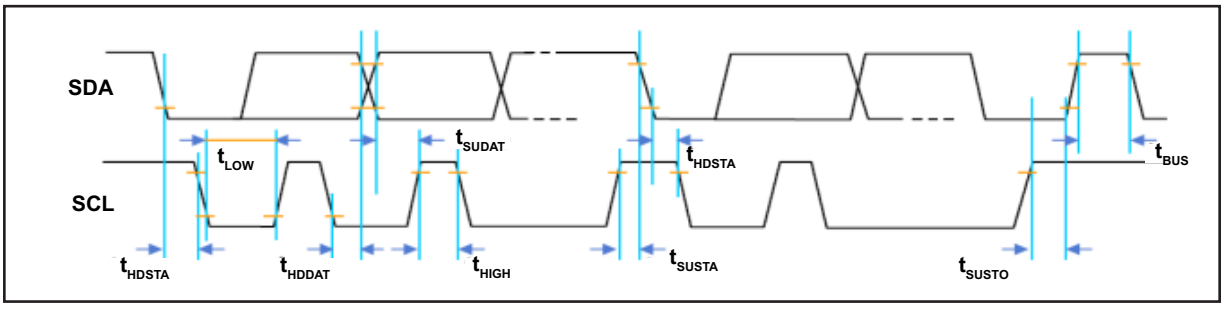


Figure 11: I²C Timing Diagram

4.2 I²C Features and Timing (cont.)

Table 8: I²C Parameters

Parameter	Symbol	Min	Typ	Max	Units
SCL clock frequency	f_{SCL}	20		400	kHz
Start condition hold time relative to SCL edge	t_{HDSTA}	0.1			µs
Minimum SCL clock low width [1]	t_{LOW}	0.6			µs
Minimum SCL clock high width [1]	t_{HIGH}	0.6			µs
Start condition setup time relative to SCL edge	t_{SUSTA}	0.1			µs
Data hold time on SDA relative to SCL edge	t_{HDDAT}	0		0.5	µs
Data setup time on SDA relative to SCL edge	t_{SUDAT}	0.1			µs
Stop condition setup time on SCL	t_{SUSTO}	0.1			µs
Bus free time between stop condition and start condition	t_{BUS}	1			µs

1. Combined low and high widths must equal or exceed minimum SCL period.

4.3 Measurement Modes

The ChipCap 2 can be programmed to operate in either Sleep Mode or Update Mode. The measurement mode is selected with the Measurement_Mode bit in the ChipCap 2 Config Register word. In Sleep Mode, the part waits for commands from the master before taking measurements (see section 4.3.2 on page 15).

4.3.1 Data Fetch in Update Mode

In Update Mode, I²C is used to fetch data from the digital output register using a Data Fetch (DF) command.

Detecting when data is ready to be fetched can be handled either by polling or by monitoring the Ready pin (see section 4.8 on page 20 for details on the Ready pin). The status bits of a DF tell whether or not the data is valid or stale (see Table 9 on page 17 regarding the status bits). As shown in Figure 12 below, after a measurement cycle is complete, valid data can be fetched. If the next data fetch is performed too early, the data will be the same as the previous fetch with stale status bits. As shown in Figure 12 below, a rise on the Ready pin can also be used to tell when valid data is ready to be fetched.

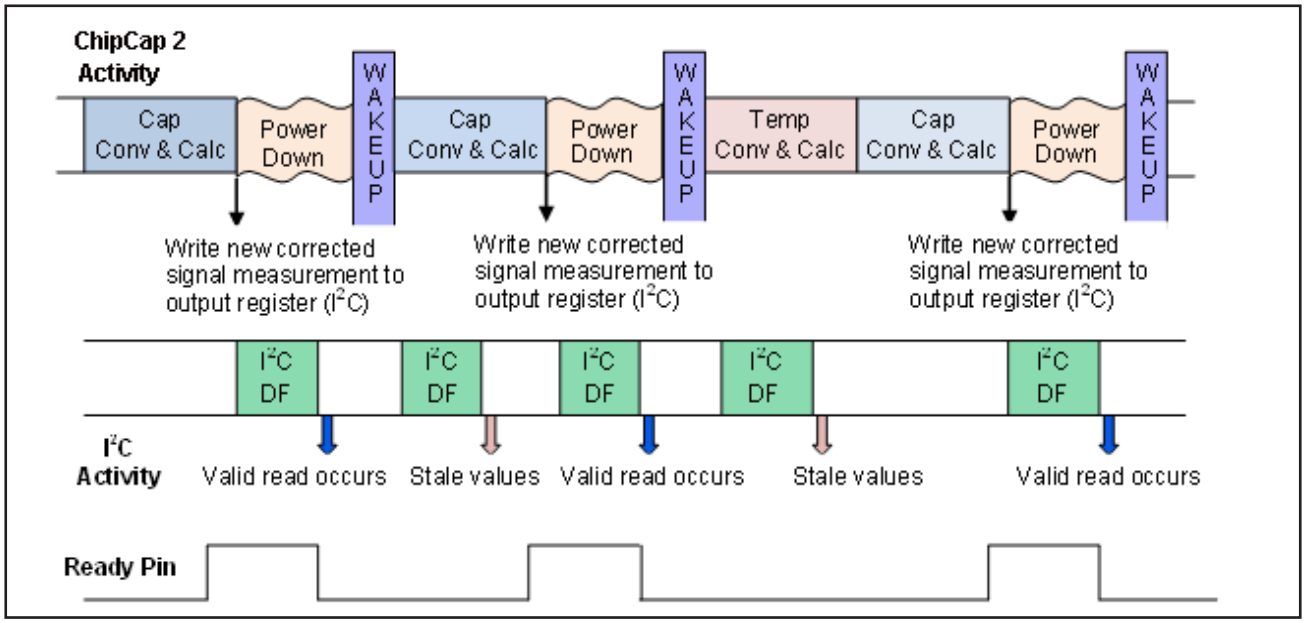


Figure 12: I²C Data Fetching in Update Mode

4.3.2 Data Fetch in Sleep Mode

In Sleep Mode, the ChipCap 2 core will only perform conversions when ChipCap 2 receives a Measurement Request command (MR); otherwise, the ChipCap 2 is always powered down. Measurement Request commands can only be sent using I²C, so Sleep Mode is *not available* for PDM. The Alarms can be used in Sleep Mode but only in combination with I²C.

Note: *Sleep Mode power consumption is significantly lower than Update Mode power consumption (see Table 5 on page 11 for exact values).*

4.3.2 Data Fetch in Sleep Mode (cont.)

Figure 13 below shows the measurement and communication sequence for Sleep Mode. The master sends an MR command to wake the ChipCap 2 from power down. After ChipCap 2 wakes up, a measurement cycle is performed consisting of both a temperature and a capacitance conversion followed by the ChipCap 2 Core correction calculations.

At the end of a measurement cycle, the digital output register and alarms will be updated before powering down. An I²C data fetch (DF) is performed during the power-down period to fetch the data from the output register. In I²C the user can send another MR to start a new measurement cycle without fetching the previous data. After the data has been fetched, the ChipCap 2 remains powered down until the master sends an MR command.

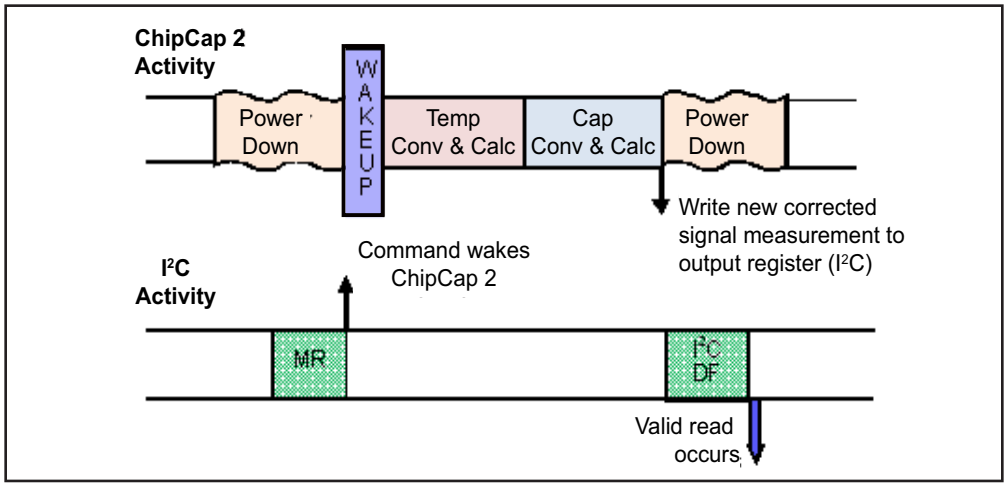


Figure 13: Measurement Sequence in Sleep Mode

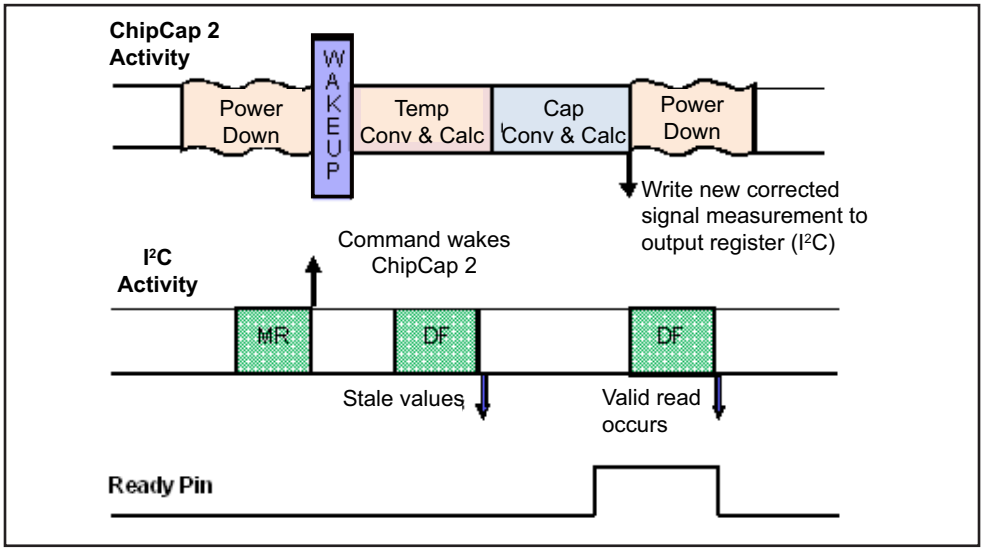


Figure 14: I²C Data Fetching in Sleep Mode

4.3.2 Data Fetch in Sleep Mode (cont.)

In Sleep Mode, I^2C are used to request a measurement with a MR command and to fetch data from the digital output register using a Data Fetch (DF) command (see section 4.7 on page 20 for details on the MR command).

Detecting when data is ready to be fetched can be handled either by polling or by monitoring the Ready pin (see section 4.8 on page 20 for details on the Ready pin). The status bits of a DF tell whether the data is valid or stale (see section 4.4 regarding the status bits). As shown in Figure 14 on the previous page, after a measurement cycle is complete, valid data can be fetched. If the next data fetch is performed too early, the data will be the same as the previous fetch with stale status bits. A rise on the Ready pin (Figure 14) can also be used to tell when valid data is ready to be fetched.

4.4 Status Bits

Status bits (the two MSBs of the fetched high data byte, see Table 9 below) are provided in I^2C but not in PDM. The status bits are used to indicate the current state of the fetched data.

Table 9: Status Bits

Status Bits (I^2C)	PDM Output	Definition
00B	Clipped normal output	Valid data: Data that has not been fetched since the last measurement cycle.
01B	Not applicable	Stale data: Data that has already been fetched since the last measurement cycle.
10B	Not applicable	Command Mode: The ChipCap 2 is in Command Mode.
11B	Not used	Not used

4.5 I^2C Commands

As detailed in Table 10 below, there are two types of commands which allow the user to interface with the ChipCap 2 in the I^2C.

Table 10: I^2C Command Bits

Type	Description	Communication Supported	Reference Sections
Data Fetch (DF)	Used to fetch data in any digital mode	I^2C	Section 4.6
Measurement Request (MR)	Used to start measurements in Sleep Mode	I^2C	Section 4.7

4.6 Data Fetch (DF)

The Data Fetch (DF) command is used to fetch data in any digital output mode.

An I^2C Data Fetch command starts with the 7-bit slave address and the 8th bit = 1 (READ).

The ChipCap 2 as the slave sends an acknowledgement (ACK) indicating success.

The number of data bytes returned by the ChipCap 2 is determined by when the master sends the NACK and stop condition. Figure 15 on page 19 shows examples of fetching two, three and four bytes respectively.

The full 14 bits of humidity data are fetched in the first two bytes. The MSBs of the first byte are the status bits.

If temperature data is needed, additional temperature bytes can be fetched. In Figure 15 on page 19, the three-byte data fetch returns 1 byte of temperature data (8-bit accuracy) after the humidity data. A fourth byte can be fetched where the six MSBs of the fetched byte are the six LSBs of a 14-bit temperature measurement. The last two bits of the fourth byte are undetermined and should be masked off in the application.

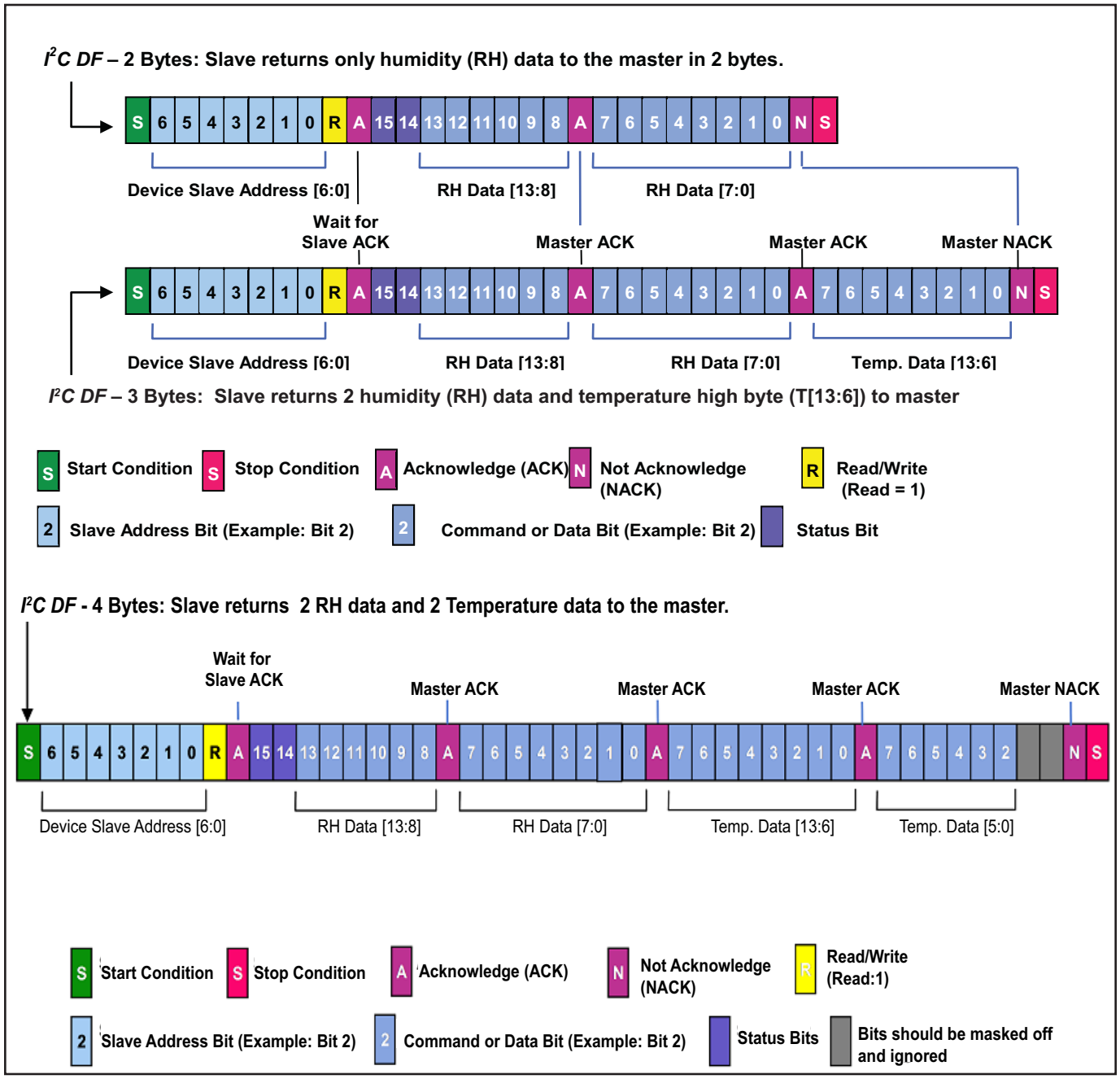


Figure 15: I²C Measurement Packet Reads

4.6 Data Fetch (DF) (cont.)

Humidity & Temperature Conversion Formula	
Humidity Output (%RH)	(RH_High [5:0] x 256 + RH_Low [7:0])/ 2^{14} x 100
Temperature Output (°C)	(Temp_High [7:0] x 64 + Temp_Low [7:2]/ 4)/ 2^{14} x 165 - 40

4.7 Measurement Request (MR)

A measurement request (MR) is a Sleep-Mode-only command sent by the master to wake up the ChipCap 2 and start a new measurement cycle in I^2C.

The I^2C MR is used to wake up the device in Sleep Mode and start a complete measurement cycle starting with a temperature measurement, followed by a humidity measurement, and then the results can be fetched by master with I^2C.

As shown in Figure 16 below, the communication contains only the slave address and the WRITE bit (0) sent by the master.

After the ChipCap 2 responds with the slave ACK, the master creates a stop condition.

Note: *The I^2C MR function can also be accomplished by sending "don't care" data after the address instead of immediately sending a stop bit.*

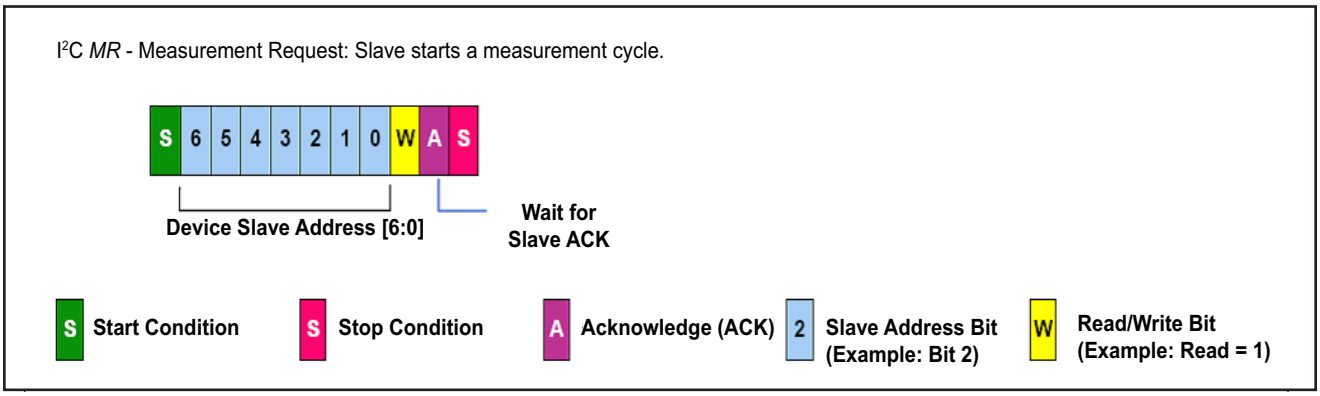


Figure 16: I²C Measurement Request

4.8 Ready Pin

A rise on the Ready pin indicates that new data is ready to be fetched from the I^2C interface. The Ready pin stays high until a Data Fetch (DF) command is sent; it stays high even if additional measurements are performed before the DF.

The Ready pin's output driver type is selectable as either full push-pull or open drain using the Ready_Open_Drain bit in EEPROM word Cust_Config (see Table 16 on page 32 for bit assignments and settings). Point-to-point communication most likely uses the full push-pull driver. If an application requires interfacing to multiple parts, then the open drain option can allow for just one wire and one pull-up resistor to connect all the parts in a bus format.

4.9 Command Mode

Command Mode commands are only supported for the I²C protocol. As shown in Figure 17 below, commands are 4-byte packets with the first byte being a 7-bit slave address followed by 0 for write. The second byte is the command byte and the last two bytes form a 16-bit data field.

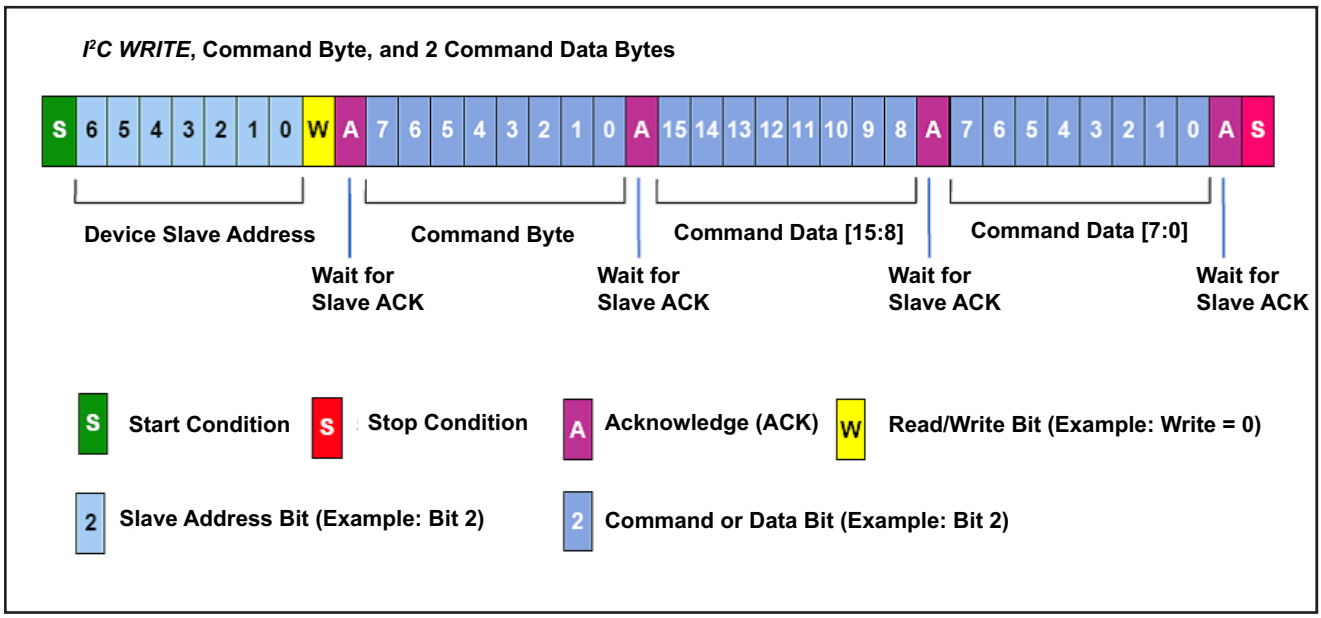


Figure 17: I²C Command Format

4.10 Command Encodings

Table 11 describes all the commands that are offered in Command Mode.

Note: *Only the commands listed in Table 11 are valid. Other encodings might cause unpredictable results. If data is not needed for the command, zeros must be supplied as data to complete the 4-byte packet.*

Table 11: Command List and Encodings

Command Byte 8 Command Bits (Hex)	Third and Fourth Bytes 16 Data Bits (Hex)	Description	Response Time
0x16 to 0x1F	0x0000	EEPROM Read of addresses 0x16 to 0x1F After this command has been sent and executed, a data fetch must be performed.	100µs
0x56 0x5F	0xYYYY (Y = data)	Write to EEPROM addresses 0x16 to 0x1F The 2 bytes of data sent will be written to the address specified in the 6 LSBs of the command byte	12ms
0x80	0x0000	Start_NOM Ends Command Mode and transitions to Normal Operation Mode.	
0xA0	0x0000	Start_CM Start Command Mode: used to enter the command interpreting mode. Start_CM is only valid during the power-on command window.	100µs

4.11 Command Response and Data Fetch

After a command has been sent and the execution time defined in Table 11 has expired, an I^2C Data Fetch (DF) can be performed to fetch the response. As shown in Figure 18 on page 24, after the slave address has been sent, the first byte fetched is the response byte.

The upper two status bits will always be 10 to represent Command Mode. The lower two bits are the response bits. Table 12 on page 23 describes the different responses that can be fetched. To determine if a command has finished executing, poll the part until a Busy response is no longer received. The middle four bits of the response byte are command diagnostic bits where each bit represents a different diagnostic (see Table 13 on page 23).

Note: *Regardless of what the response bits are, one or more of the diagnostic bits may be set indicating an error occurred during the execution of the command.*

Note: *Only one command can be executed at a time. After a command is sent another command must not be sent until the execution time of the first command defined in Table 11 above has expired*.

4.11 Command Response and Data Fetch (cont.)

For all commands except EEPROM Read and Get Revision, the data fetch should be terminated after the response byte is read. If the command was a Get Revision, then the user will fetch a one byte Revision as shown in Figure 18 on page 24, example 2.

The revision is coded with the upper nibble being the letter corresponding to a full layer change and the lower nibble being the metal change number, for example A0. If the command was an EEPROM Read, then the user will fetch two more bytes as shown in Figure 18 on page 24, example 3.

If a Corrected EEPROM Error diagnostic was flagged after an EEPROM read, the user has the option to write this data back to attempt to fix the error. Instead of polling to determine if a command has finished executing, the user can use the Ready pin. In this case, wait for the Ready pin to rise, which indicates that the command has executed. Then a data fetch can be performed to get the response and data (see Figure 18 on page 24).

Table 12: Response Bits

Encoding	Name	Description
00	Busy	The command is busy executing.
01	Positive Acknowledge	The command executed successfully.
10	Negative Acknowledge	The command was not recognized or an EEPROM write was attempted while the EEPROM was locked.

Table 13: Command Diagnostic Bits

Bit Position	Name	Description
2	Corrected EEPROM Error	A corrected EEPROM error occurred in execution of the last command.
3	Uncorrectable EEPROM Error	An uncorrectable EEPROM error occurred in execution of the last command.
4	RAM Parity Error	A RAM parity error occurred during a microcontroller instruction in the execution of the last command.
5	Configuration Error	An EEPROM or RAM parity error occurred in the initial loading of the configuration registers.

4.11 Command Response and Data Fetch (cont.)

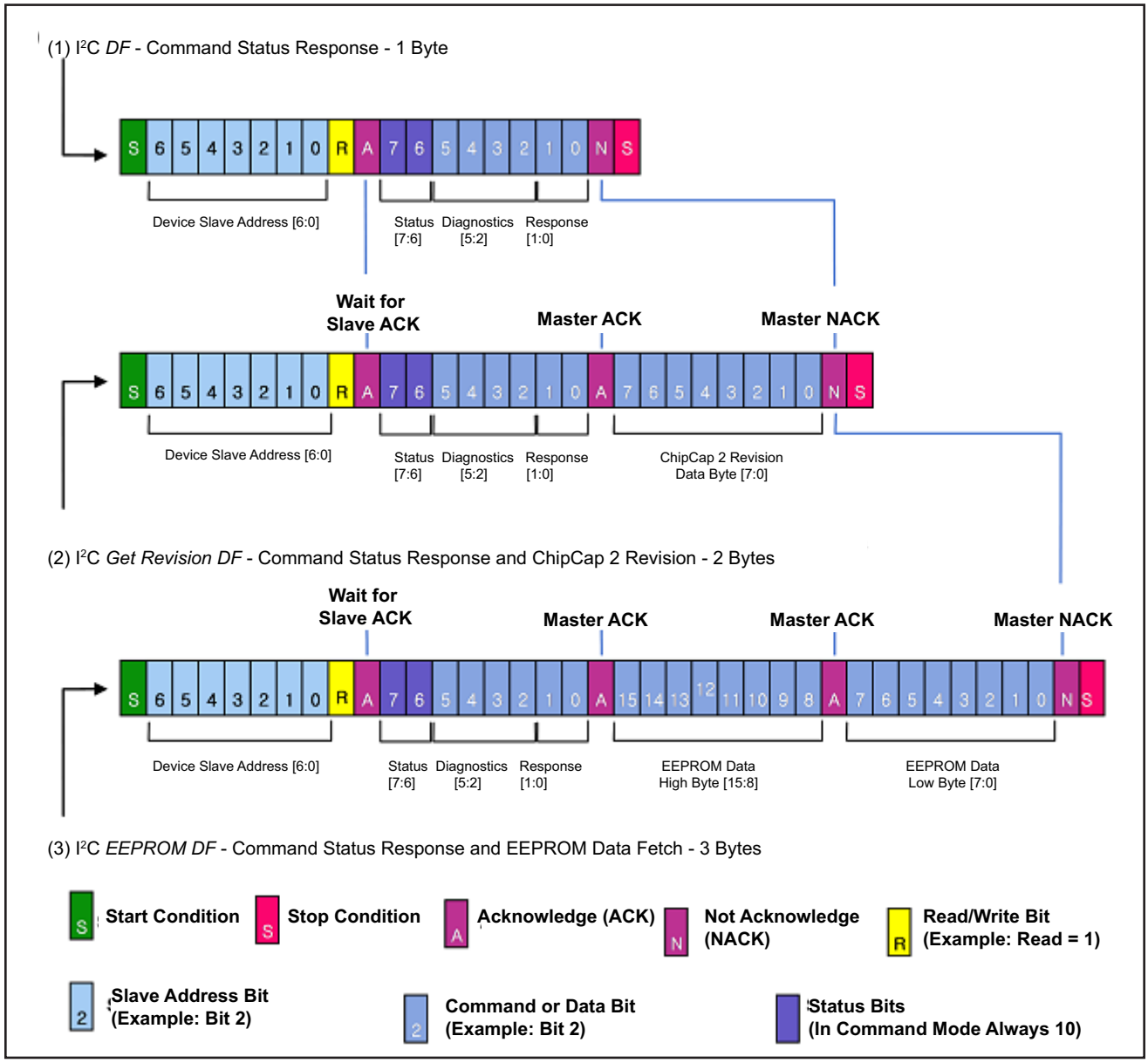


Figure 18: Command Mode Data Fetch

4.12 EEPROM

The EEPROM array contains the calibration coefficients for gain and offset, etc., and the configuration bits for the analog front end, output modes, measurement modes, etc. The ChipCap 2 EEPROM is arranged as 10 16-bit words (see Table 14 on page 25).

See section 4.9, “Command Mode” on page 21, for instructions on reading and writing to the EEPROM in Command Mode via the I^{2}C interface. When programming the EEPROM, an internal charge pump voltage is used; therefore, a high voltage supply is not needed.

Table 14: EEPROM Word Assignments

EEPROM Word	Bit Range	IC Default	Name	Description and Notes
16_{HEX}	13:0	0x3FFF	PDM_Clip_High	PDM high clipping limit
17_{HEX}	13:0	0x0000	PDM_Clip_Low	PDM low clipping limit
18_{HEX}	13:0	0x3FFF	Alarm_High_On	High alarm on trip point
19_{HEX}	13:0	0x3FFF	Alarm_High_Off	High alarm off trip point
$1A_{HEX}$	13:0	0x0000	Alarm_Low_On	Low alarm on trip point
$1B_{HEX}$	13:0	0x0000	Alarm_Low_Off	Low alarm off trip point
$1C_{HEX}$	15:0	0x0028	Cust_Config	Customer Configuration (see Table 16 on page 32)
$1D_{HEX}$	15:0	0x0000	Reserved	Reserved Word: **Do Not Change**; must leave at factory settings
$1E_{HEX}$	15:0	0x0000	Cust_ID2	Customer ID byte 2: For use by customer
$1F_{HEX}$	15:0	0x0000	Cust_ID3	Customer ID byte 3: For use by customer

5. Converting PDM to Analog Signal

5.1 PDM (Pulse Density Modulation)

Both corrected humidity and temperature are available in PDM output. Humidity PDM appears on PDM_H (2) pad and Temperature PDM appears on the PDM_T (1) pad.

The PDM frequency is 231.25 kHz ±15% (i.e., the oscillator frequency 1.85 MHz ±15% divided by 8). Both PDMs output 14-bit values for Humidity and Temperature.

In PDM Mode, ChipCap 2 is programmed to Update Mode. Every time a conversion cycle has finished, the PDM will begin outputting the new value.

See Figure 19 below for the PDM Timing Diagram.

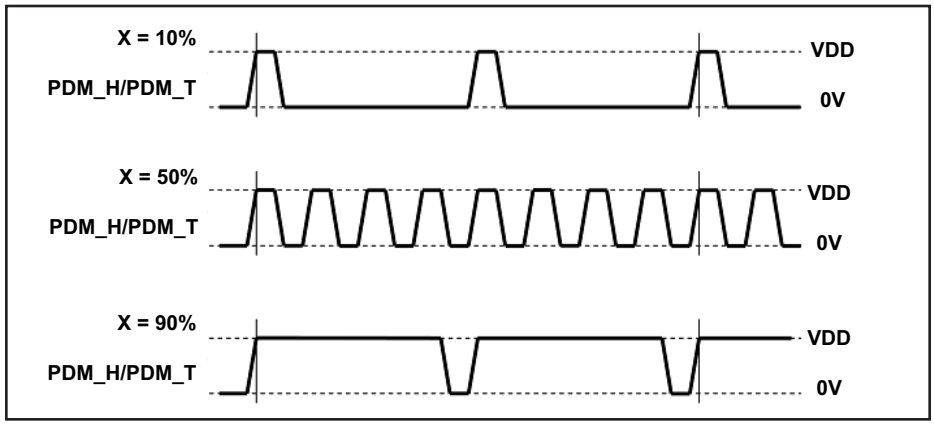


Figure 19: PDM Signal Timing Diagram

5.2 Low Pass Filtering

An analog output value is created by low-pass filtering the PDM output; a simple first-order RC filter will work in this application.

Select the time constant of the filter based on the requirements for setting time and/or peak-to-peak ripple.

IMPORTANT: *The resistor of the RC filter must be ≥10 kΩ.*

Table 15: Low Pass Filter Example for R=10 kΩ

Filter Capacitance (nF)	PDM_H / PDM_T		Desired Analog Output Resolution
	Vpp Ripple (mV/V)	0 to 90% settling time (ms)	
100	4.3	2.3	8
400	1.0	9.2	10
1600	0.3	36.8	12
6400	0.1	147.2	14

5.2 Low Pass Filtering (cont.)

For a different (higher) resistor, the normalized ripple VPP (mV/V) can be calculated as:

VPP (mV/V) = 4324 / [R(kΩ) * C(nF)]

Or the setting time t_{SETT} for a 0% to 90% setting can be calculated as:

t_{SETT} (ms) = 0.0023 * R(kΩ) * C(nF)

5.3 Analog Output Characteristics

5.3.1 Polynomial Equation Humidity

PDM_H [mV]= %RH /100 * VDD[mV]

5.3.2 Polynomial Equation Temperature

PDM_T [mV] = ((T[°C] / 165) +0.2424)*VDD[mV]

6. Alarm Function (Optional)

6.1 Alarm Output

The alarm output can be used to monitor whether the Humidity reading has exceeded or fallen below pre-programmed values. The alarm can be used to drive an open-drain load connected to VDD as shown in Figure 22 on page 30 or it can function as a full push-pull driver. If a high voltage application is required, external devices can be controlled with the Alarm pads, as demonstrated in Figure 20 on page 29 and Figure 21 on page 30.

In standard ChipCap 2 PDM mode, only the High Alarm can be used.

6.2 Alarm Registers

Four registers are associated with the alarm functions: Alarm_High_On, Alarm_High_Off, Alarm_Low_On, and Alarm_Low_Off (see Table 14 on page 25 for EEPROM addresses). Each of these four registers is a 14-bit value that determines where the alarms turn on or off. The two high alarm registers form the output with hysteresis for the Alarm_High pin, and the two low alarm registers form the output with hysteresis for the Alarm_Low pin. Each of the two alarm pins can be configured independently using Alarm_Low_Cfg and Alarm_High_Cfg located in EEPROM word Cust_Config (see Table 16 on page 32 for bit assignments).

Note: *If two high alarms or two low alarms are needed, see the section Alarm Polarity on the next page*.

6.3 Alarm Operation

As shown in Figure 23 on page 31, the Alarm_High_On register determines where the high alarm trip point is and the Alarm_High_Off register determines where the high alarm turns off if the high alarm has been activated. The high alarm hysteresis value is equal to Alarm_High_On - Alarm_High_Off. The same is true for the low alarm where Alarm_Low_On is the low alarm trip point with Alarm_Low_Off determining the alarm shut off point. The low alarm hysteresis value is equal to Alarm_Low_Off - Alarm_Low_On. Figure 24 on page 31 shows output operation flowcharts for both the Alarm_High and Alarm_Low pins.

6.4 Alarm Output Configuration

The user can select the output driver configuration for each alarm using the Output Configuration bit in the Alarm_High_Cfg and Alarm_Low_Cfg registers in EEPROM word Cust_Config (see Table 16 on page 32 for bit assignments). For applications, such as interfacing with a microcontroller or controlling an external device, select the full push-pull driver for the alarm output type. For an application that directly drives a load connected to VDD, the typical selection is the open-drain output type. An advantage of making an alarm output open drain is that in a system with multiple devices, the alarm outputs of each ChipCap 2 can be connected together with a single pull-up resistance so that one can detect an alarm on any device with a single wire.

6.5 Alarm Polarity

For both alarm pins, the polarity of the alarm output is selected using the Alarm Polarity bit in the Alarm_High_Cfg and Alarm_Low_Cfg registers in EEPROM word Cust_Config (see Table 16 on page 32 for bit assignments). Another feature of the polarity bits is the ability to create two high alarms or two low alarms. For example, with applications requiring two high alarms, flip the polarity bit of the Alarm_Low pin, and it will act as a high alarm.

However, in this case, the effect of the alarm low registers is also changed: the Alarm_Low_On register would act like the Alarm_High_Off register and the Alarm_Low_Off register would act like the Alarm_High_On register. The same can be done to achieve two low alarms: the Alarm_High pin would have the polarity bit flipped, and the two Alarm_High registers would have opposite meanings.

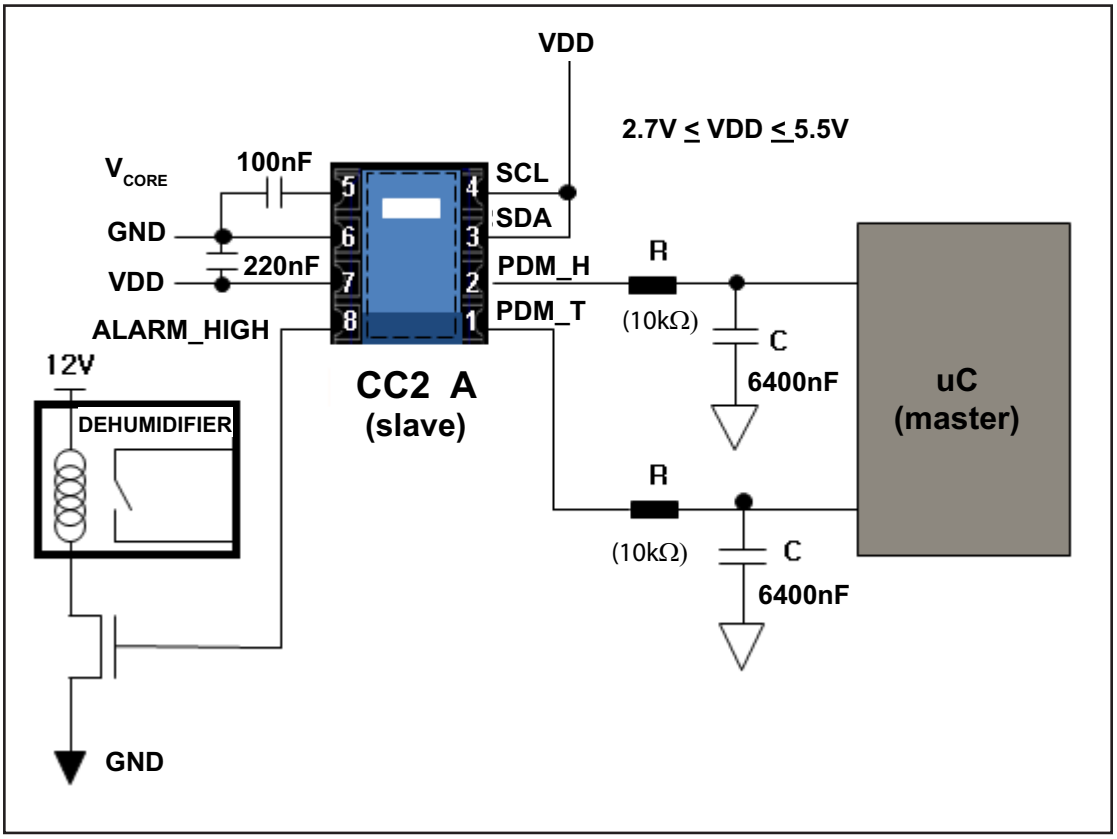


Figure 20: Bang-Bang Humidity Control (High Voltage Application): ChipCap 2 PDM: 1 Alarm/Humidity Output (Optional)

6.5 Alarm Polarity (cont.)

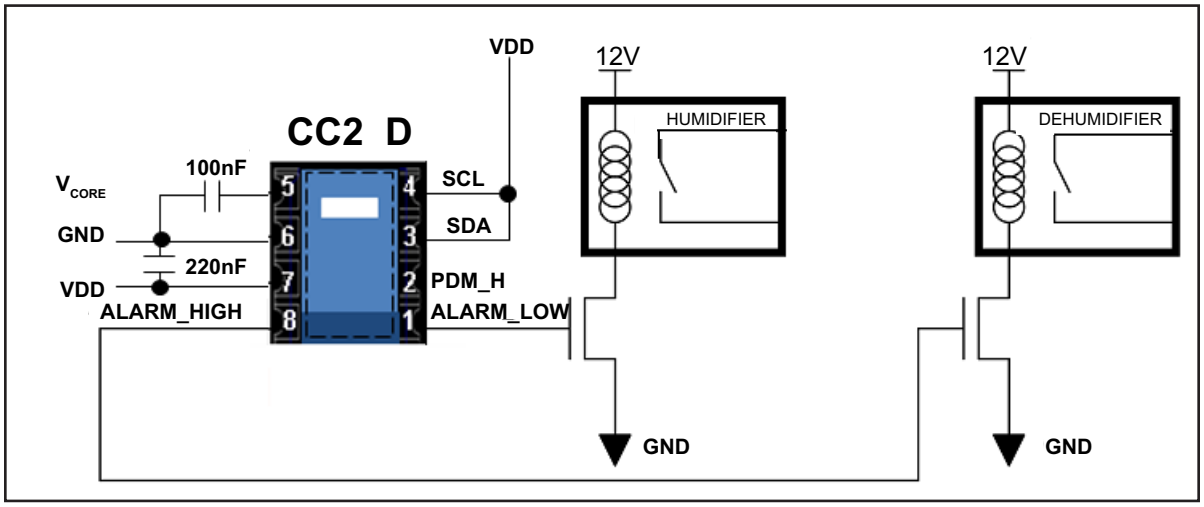


Figure 21: Bang-Bang Humidity Control (High Voltage Application):
ChipCap 2 I^2C:2 Alarms / Humidity Output (Optional)

ChipCap 2 also can be directly installed to a device without MCU interface when only a switch on/off function is required at the desired humidity level (e.g., bathroom vent fan, humidifiers, dehumidifiers).

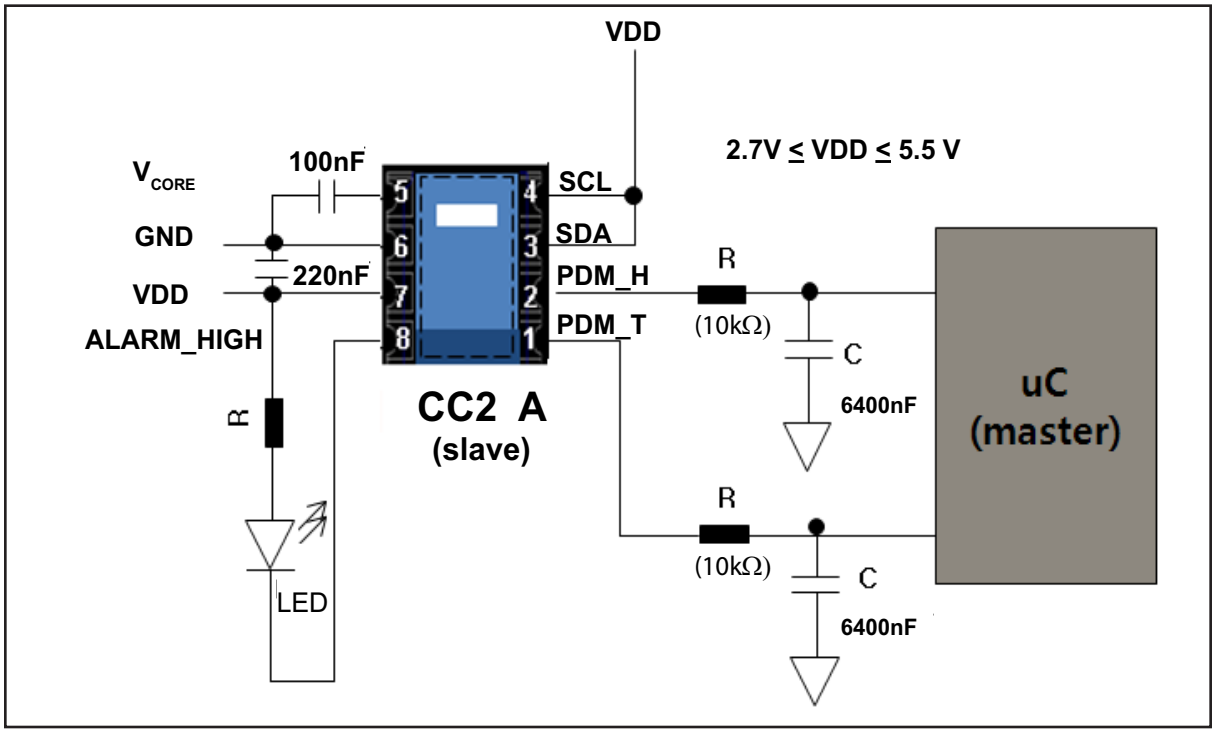


Figure 22: LED control with Alarm Function
ChipCap 2 PDM: 1 Alarm/ Humidity Output (Optional)

6.5 Alarm Polarity (cont.)

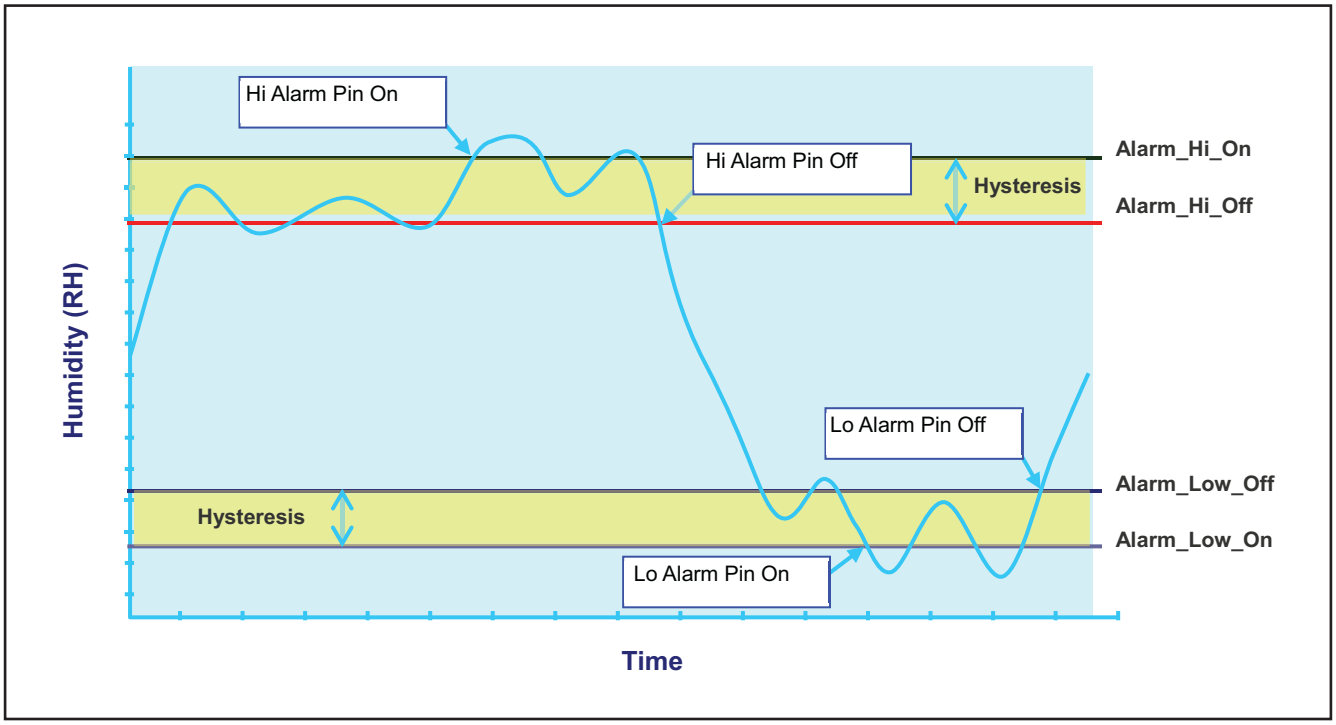


Figure 23: Example of Alarm Function

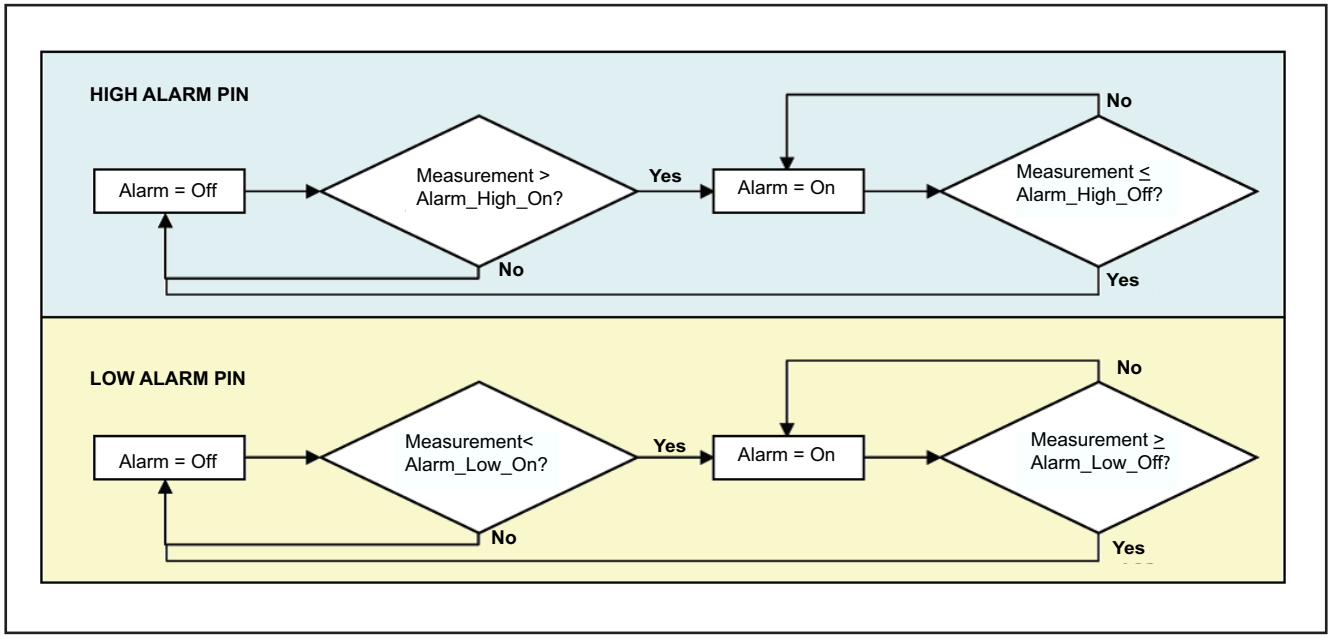


Figure 24: Alarm Output Flow Chart

6.5 Alarm Polarity (cont.)

Table 16: Cust_Config Bit Assignments

<table>
<tr><th>Bit Range</th><th>IC Default</th><th>Name</th><th>Description and Notes</th></tr>
<tr><td>6:0</td><td>0101000</td><td>Device_ID</td><td>I^2C slave address</td></tr>
<tr><td>8:7</td><td>00</td><td>Alarm_Low_Cfg</td><td>Configure the Alarm_Low output pin:
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>7</td><td>Alarm Polarity
0 = Active High
1 = Active Low</td></tr><tr><td>8</td><td>Output Configuration
0 = Full push-pull
1 = Open Drain</td></tr></table></td></tr>
<tr><td>10:9</td><td>00</td><td>Alarm_High_Cfg</td><td>Configure the Alarm_High output pin:
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>9</td><td>Alarm Polarity
0 = Active High
1 = Active Low</td></tr><tr><td>10</td><td>Output Configuration
0 = Full push-pull
1 = Open Drain</td></tr></table></td></tr>
<tr><td>*12</td><td>0</td><td>Ready_Open_Drain</td><td>Ready pin is
0 = Full push-pull
1 = Open drain</td></tr>
<tr><td>*13</td><td>0</td><td>Fast_Startup</td><td>Sets the Command Window length:
0 = 10 ms Command Window
1 = 3 ms Command Window</td></tr>
<tr><td>15:14</td><td>00</td><td>Reserved</td><td>Do Not Change - must leave at factory settings</td></tr>
</table>

** Only applies to I^2C output.*

7. Part Number List

Table 17: Part Number List

GE part no.	Description
CC2A25	ChipCap2, analog, 2%, 5v
CC2A23	ChipCap2, analog, 2%, 3.3v
CC2D23S	ChipCap2, digital, sleep mode, 2%, 3.3v
CC2D25S	ChipCap2, digital, sleep mode, 2%, 5v
CC2D23	ChipCap2, digital, 2%, 3.3v
CC2D25	ChipCap2, digital, 2%, 5v
CC2D35	ChipCap2, digital, 3%, 5v
CC2A33	ChipCap2, analog, 3%, 3.3v
CC2D33S	ChipCap2, digital, sleep mode, 3%, 3.3v
CC2D35S	ChipCap2, digital, sleep mode, 3%, 5v
CC2D33	ChipCap2, digital, 3%, 3.3v
CC2A35	ChipCap2, analog, 3%, 5v

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